Claims PTO
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AMW

Claims 1-15 cancelled.

16. A TFT substrate, comprising:

a gate electrode comprising a first metal film over a substrate and a second metal film over the first metal film;

a gate pad consisting the first metal film and a portion of a removed area of the second metal film;

an insulated film over the gate electrode and having an exposed area of the first metal film over the gate pad;

a semiconductor film pattern over the insulated film;

a source electrode formed over a first portion of the semiconductor film pattern;

a drain electrode formed over a second portion of the semiconductor film pattern;

a passivation film pattern formed over the source electrode, having a contact hole over the drain electrode and having an exposed area of the first metal film of the gate pad;

a first pixel electrode pattern electrically contacted to the drain electrode on the passivation film pattern; and

a second pixel electrode pattern electrically contacted to the exposed area of the first metal film of the gate pad.

17. A TFT substrate, as recited in claim 16, wherein the first metal film comprises a refractory metal.

18. A TFT substrate, as recited in claim 17, wherein the first metal film comprises a material selected from the group consisting of CR, Ta, Mo, and Ti.

19. A TFT substrate, as recited in claim 16, wherein the second metal film comprises Al or an Al alloy.

20. A TFT substrate, as recited in claim 16, wherein the insulated film comprises a nitride film SiN.

21. A TFT substrate, as recited in claim 16, wherein the first and second pixel patterns comprise ITO.

22. A TFT substrate, as recited in claim 16, wherein a portion of the passivation film directly contacts the semiconductor film pattern.

Claims 23-28 cancelled.

29. A TFT substrate, as recited in claim 16, wherein a portion of the passivation film directly contacts the semiconductor film pattern.

Claims 30-37 cancelled.

37. A method for manufacturing a liquid crystal display as in claim 8, wherein the second pixel electrode pattern contacts portions of the exposed gate pad.

38. A TFT substrate as in claim 16, wherein at least one of the first and the second metal film of the gate electrode and the gate pad has tapered-sidewalls.

39. A TFT substrate as in claim 38, wherein the second metal film has tapered sidewalls.

40. A TFT substrate as in claim 16, wherein the semiconductor film pattern comprises:

an amorphous silicon film on the insulated film; and

a doped amorphous silicon film on the amorphous silicon film.

41. A TFT substrate as in claim 16, wherein the second pixel electrode pattern contacts portions of the exposed gate pad.

Claims 42-49 cancelled.